كلية مدينة العلم الجامعة
قسم هندسة الحاسوب

محاضرات المرحلة الاولى لمادة الهندسة الالكترونية

اعداد

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DC Biasing

المحاضرة الرابعة

References

Text Books :

1-ELECTRONIC DEVICES AND CIRCUIT THEORY
Eleventh Edition By
Robert L. Boylestad and Louis Nashelsky

2-ELECTRONIC DEVICES
Ninth Edition By
Thomas L. Floyd

DC Biasing

Purpose of the DC biasing circuit

- **To turn the device "ON"**
- **To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of I_B, I_C, and V_{CE}**

DC Biasing

The biasing circuit can be designed to set the device operation at any of these points or others within the *active region.*

For the BJT (npn) to be biased in its linear (or active operating region) the following must be true:

1. The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.

$$V_B > V_E$$

2. The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

$$V_B < V_C$$

[Note that for forward bias the voltage across the p–n junction is p - positive, whereas for reverse bias it is opposite (reverse) with n -positive.]

DC Biasing

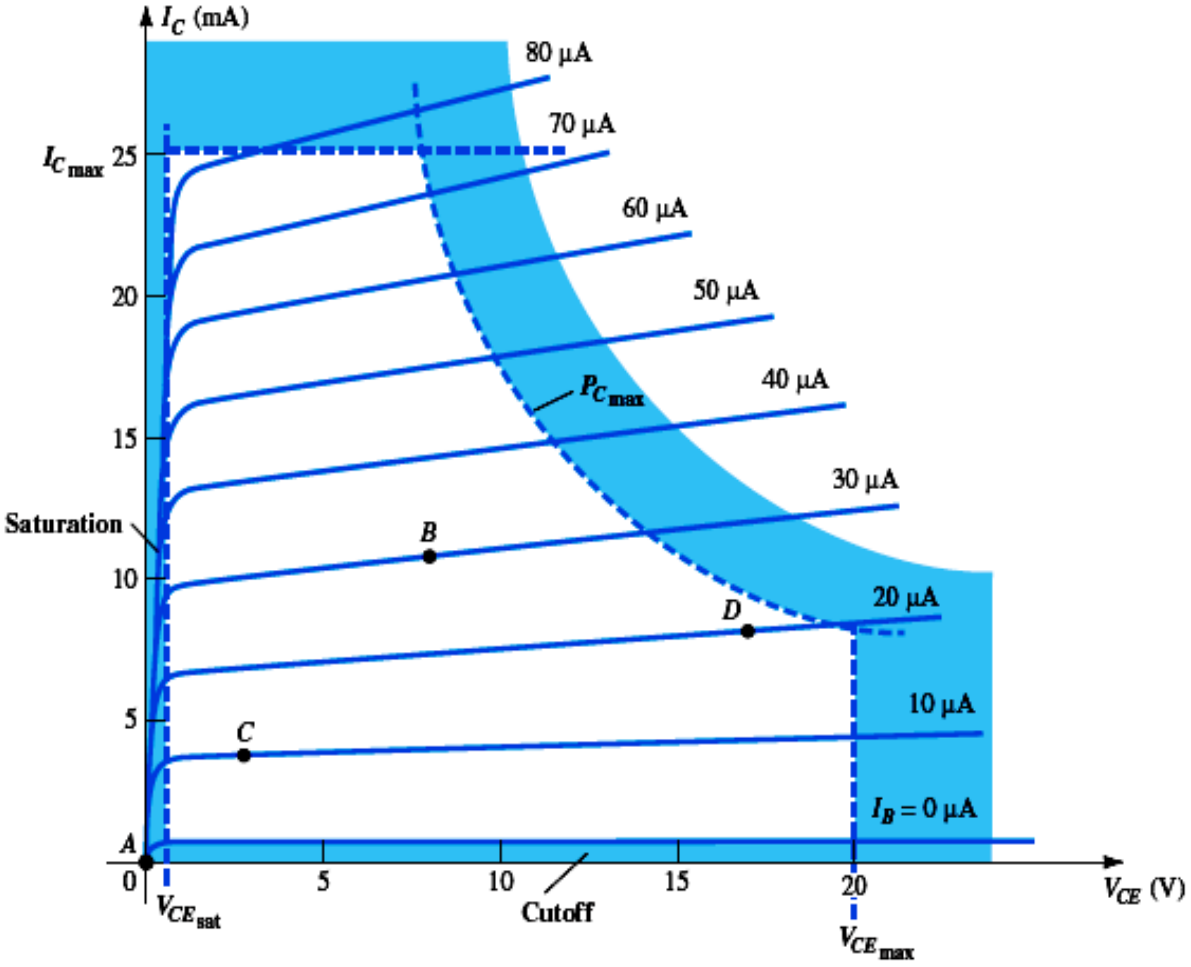


FIG. 4.1

Various operating points within the limits of operation of a transistor.

DC Biasing

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. ***Linear-region operation: See fig 4.1***

Base–emitter junction forward-biased $V_B > V_E$

Base–collector junction reverse-biased $V_B < V_C$

2. Cutoff-region operation: See fig 4.1 $I_C \cong 0$

Base–emitter junction reverse-biased $V_B < V_E$

Base–collector junction reverse-biased $V_B < V_C$

3. Saturation-region operation: See fig 4.1 $V_{CE} \cong 0$

Base–emitter junction forward-biase $V_B > V_E$

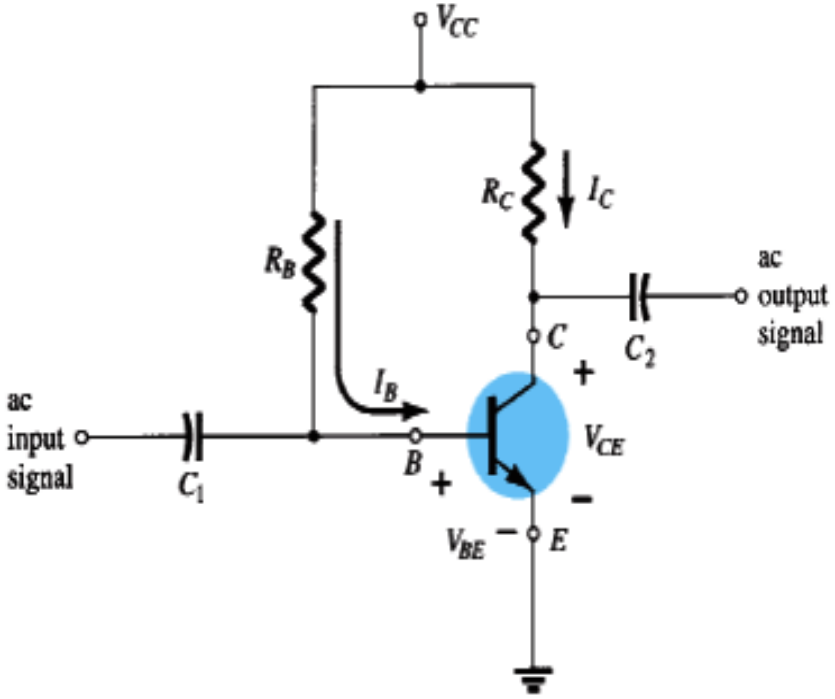
Base–collector junction forward-biased $V_B > V_C$

mode	*condition*
Active	$V_B > V_E$ $V_B < V_C$
Cutoff-region	$V_B < V_E$ $V_B < V_C$
Saturation-region	$V_B > V_E$ $V_B > V_C$

DC Biasing

1-FIXED-BIAS CONFIGURATION

The fixed-bias circuit of the Fig. below is the simplest transistor dc bias configuration. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor is a function of the applied frequency. For dc, $f = 0$ Hz, and $X_C = 1/2\pi fc = 1/2\pi(0)c = \infty$



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Base–Emitter circuit loop

Consider first the base–emitter circuit loop . Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = (V_{CC} - V_{BE}) / R_B$$

The selection of a base resistor R_B sets the level of base current for the operating point.

Collector–Emitter Loop

In the collector–emitter section of the network . The magnitude of the collector current is related directly to I_B through :

$$I_C = \beta \times I_B$$

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of collector results in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

And

$$V_{CE} = V_{CC} - I_C R_C$$

DC Biasing

which states that the voltage across the collector–emitter region of a transistor in the fixed bias configuration is the supply voltage less the drop across R_C.

$$V_{CE} = V_C - V_E$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively. *In this case,* since

$$V_E = 0 \text{ V}$$

we have

$$V_{CE} = V_C$$

In addition, because

$$V_{BE} = V_B - V_E$$

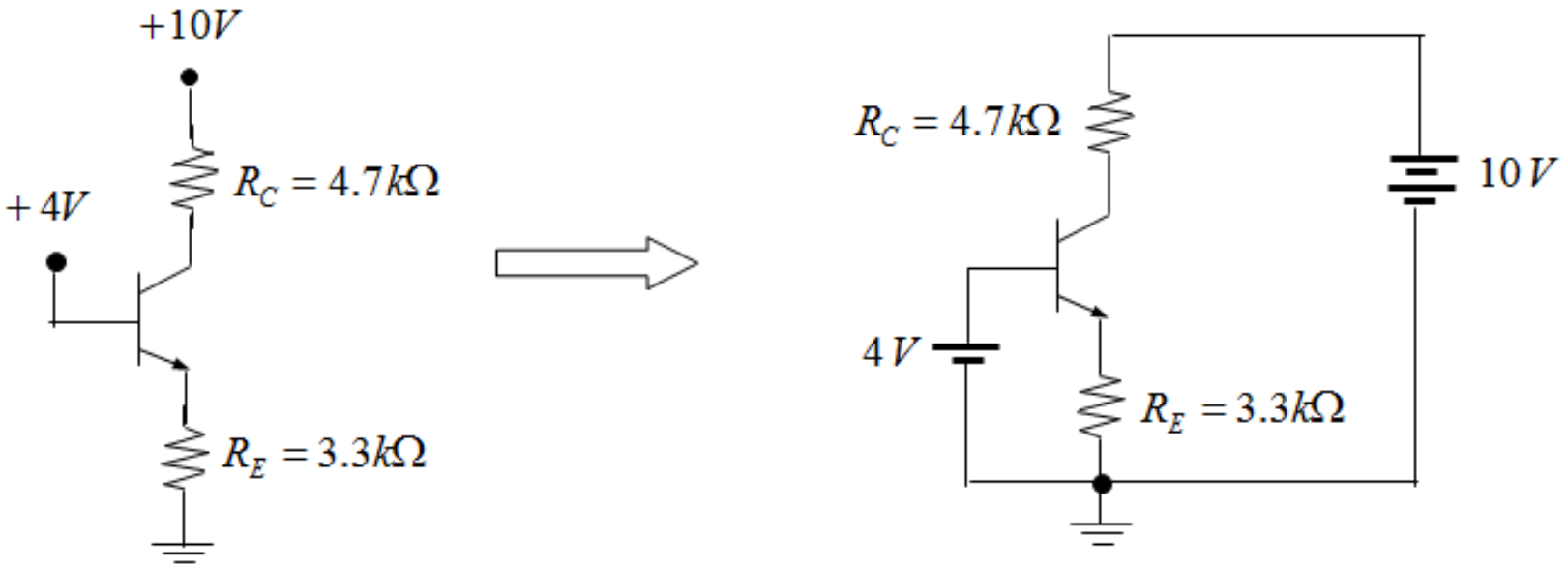
and $V_E = 0$ V,

then $V_{BE} = V_B$

DC Biasing

Example 1

We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that β is specified to be 100.

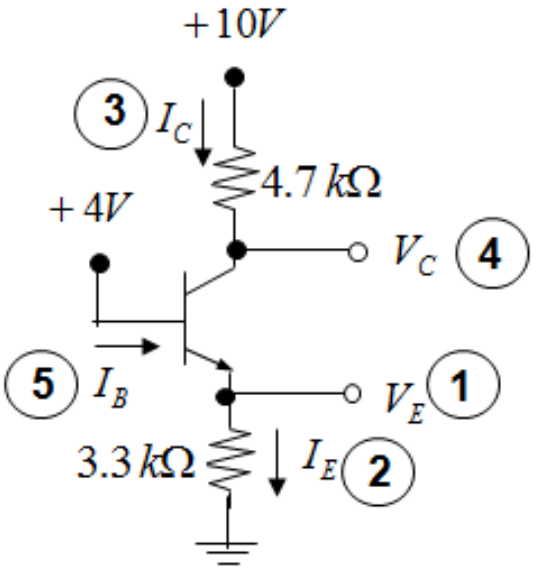


We don't know whether the transistor is in the active mode or not.

A simple approach would be to assume that the device is in the active mode, and then check our results at the end

DC Biasing

Solution



1

$$V_E = 4 - V_{BE} \approx 4 - 0.7 = 3.3\,V$$

2

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1\,mA$$

$$I_C = \alpha I_E,\ \alpha = \frac{\beta}{\beta+1} = \frac{100}{10} \approx 0.99$$

3

$$I_C = 0.99 \times 1 = 0.99\,mA$$

4

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 = +5.3\,V$$

5

$$I_B = \frac{I_E}{\beta+1} = \frac{1}{101} \approx 0.01\,mA$$

1 . V_B = 4V And > $V_E = I_E \times R_E$ = 1 mA × 3.3 KΩ = 3.3V

2. VB (= 4V) < VC (= 5.3)

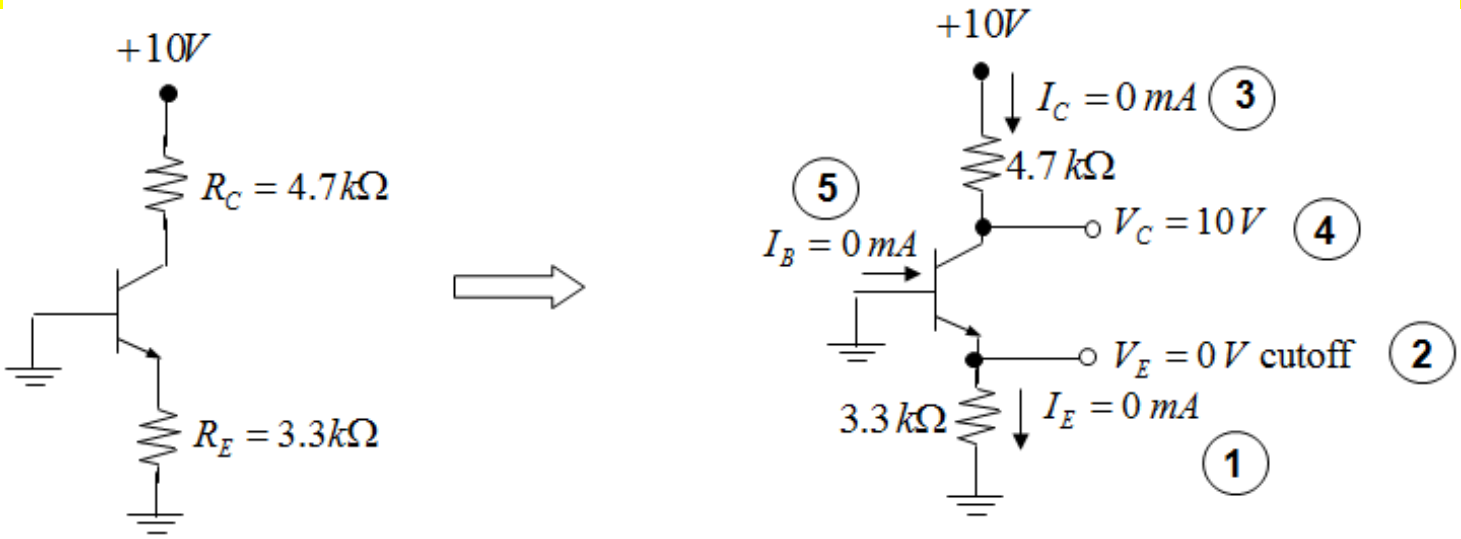
Therefore the circuit operates in active mode

DC Biasing

Example 2

We wish to analyze the circuit below to determine the voltages at all nodes and the currents through all branches. This circuit is identical to that considered in the previous two examples except that now the base voltage is zero.

Solution



1 . $V_B = 0\ V = V_E = I_E \times R_E = 0\ V$ (cutoff)

2. V_B (= 0) < VC (= 10V) (reversed biased)

Therefore the circuit operates in cutoff mode

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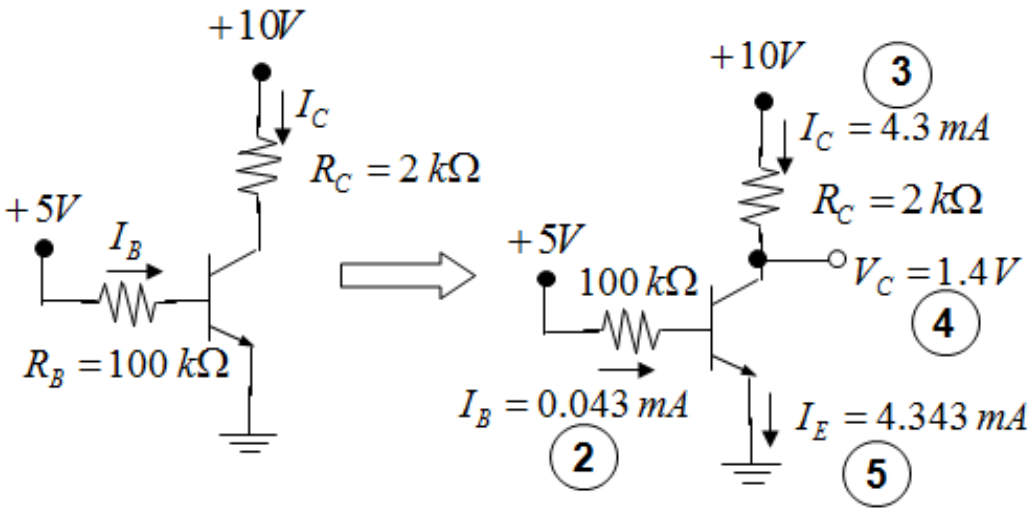
Example 3
We will analyze the following circuit to determine the voltages at all nodes and currents through all branches. Assume β=100.



$$V_B = V_{BE} \approx 0.7\,V \quad (1)$$

$$I_B = \frac{5 - V_{BE}}{R_B} \approx \frac{5 - 0.7}{100} = 0.043\,mA \quad (2)$$

$$I_C = \beta I_B = 100 \times 0.043 = 4.3\,mA \quad (3)$$

$$V_C = 10 - I_C R_C = 10 - 4.3 \times 2 = 1.4\,V \quad (4)$$

$$I_E = (\beta + 1) I_B = 101 \times 0.043 \approx 4.3\,mA \quad (5)$$

Solution

1 . $V_B = 5V > V_E (= 0.7V)$ Forward

2. $V_B = 5V > V_C (= 1.4V)$ Forward

Therefore the circuit operates in Saturation mode

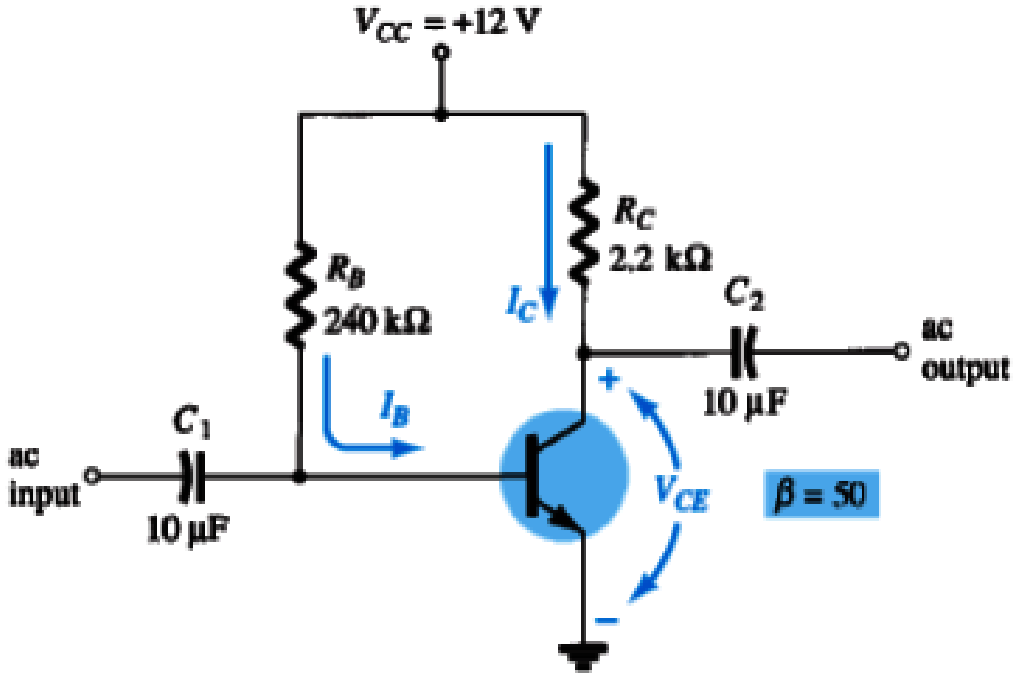
DC Biasing

Example 4

Determine the following for the fixed-bias configuration of the Fig. below

a. I_{BQ} **and** I_{CQ}. **b.** V_{CEQ}.

c. V_B **and** V_C. **d.** V_{BC}.



DC Biasing

Solution:

a. $I_{BQ} = (V_{CC} - V_{BE})/R_B = (12\ V - 0.7\ V)/240\ k\Omega = 47.08\ mA$

$I_{CQ} = \beta/I_{BQ} = (50)/(47.08\ mA) = 2.35\ mA$

b. $V_{CEQ} = V_{CC} - I_C R_C = 12\ V - (2.35\ mA)(2.2\ k\Omega) = 6.83\ V$

c. $V_B = V_{BE} = 0.7\ V$

$V_C = V_{CE} = 6.83\ V$

d. $V_{BC} = V_B - V_C = 0.7\ V - 6.83\ V = -6.13\ V$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

DC Biasing

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values.

For a transistor operating in the saturation region, the current is a maximum value *for the particular design.* Change the design and the corresponding saturation level may rise or drop.

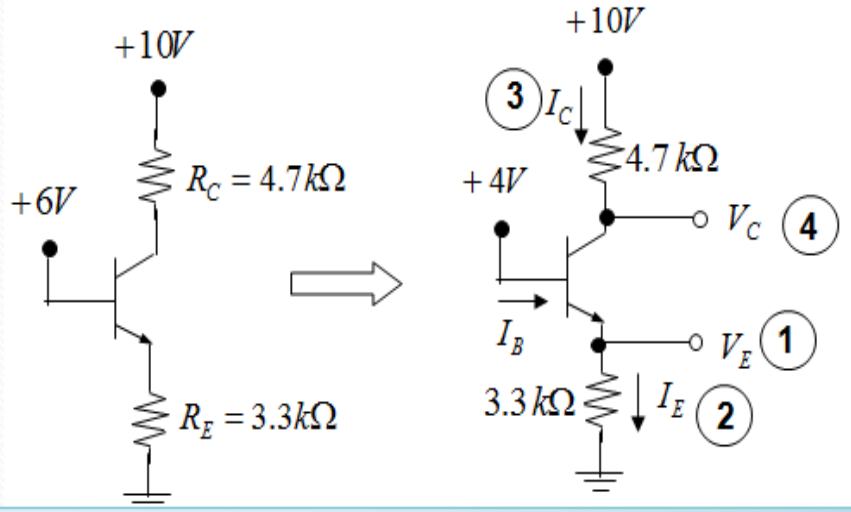
$V_B > V_E$

$V_B > V_C$

Example 5

We wish to analyze the circuit shown below to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to the previous circuit except that the voltage at the base is now +6 V.

DC Biasing



Assuming active-mode:

$$V_E = 5.6 - V_{BE} \approx 6 - 0.7 = 5.3\,V$$

$$I_E = \frac{5.3}{3.3} = 1.6\,mA$$

$$I_C = \alpha I_C \approx 1.6\,mA$$

$$V_C = 10 - 4.7 \times I_C \approx 10 - 7.52 = 2.48\,V$$

Since collector voltage > base voltage saturation mode, the transistor is not in active mode, it is in saturation mode

Example 6 :

Determine the saturation level for the network of Fig. 4.

Solution:

$I_C$sat = V_{CC} / R_C = 12 V/ 2.2 kΩ = 5.45 mA

The design of Example 4 resulted in I_{CQ} = 2.35 mA, which is far from the saturation level and about one-half the maximum value for the design.